a first lightly doped drain (LDD) region, formed in said first semiconductor layer so as to be overlapped with said first gate electrode, and

a second thin film transistor comprising:

a second semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said second semiconductor layer and a second gate electrode over said gate insulating film;

a second channel forming region formed in said second semiconductor layer;

a second source region and a second drain region formed in said second semiconductor layer; and

a second lightly doped drain (LDD) region, formed in said second semiconductor layer so as to be partially overlapped with said second gate electrode.

## REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the present application.

The Examiner's non-final Office Action dated September 13, 2001 has been received and its contents carefully noted. Claims 1-85 were pending in the present application, of which claims 45-80 are withdrawn from consideration. By this amendment, claims 1, 2, 9-11, 18-20, 27, and 36 have been amended. Accordingly, claims 1-85 remain pending, of which claims 1, 9, 18, 27, and 36 are independent.

### *Election/Restrictions*

In the Office Action, the Examiner indicated the withdrawal of claims 45-79 as being drawn to a non-elected invention. The Applicants respectfully submit that claims 45-80 are drawn to Invention II, drawn to a method of manufacturing a semiconductor device, classified in Class 438, Subclass 154 as noted in Paper No. 9. Accordingly, claims 45-80 are canceled herein without prejudice to file a divisional application directed thereto. Claims 1-44 and 81-85 remain pending.

***Drawings***

Figs. 7A, 8C, 10, 12A, 12C, 24A and 26C have been corrected in response to the objections mentioned in Paragraphs 2 and 3 of the Office Action. The Specification has also been amended in response to the objections mentioned in Paragraphs 4 and 5 of the Office Action. A Request for Approval of Drawing Corrections is filed concurrently herewith.

***Claims 1, 9, 18, 27, 36 and 81-85 are Patentable Over the AAPA and Hatano***

Claims 1, 9, 18, 27, 36 and 81-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicant's admitted prior art (AAPA) in view of Hatano et al., IEDM Technical Digest 97, pp. 523-526 (Hatano).

In this rejection, the Examiner is contending that it would have been obvious for one of ordinary skill in the art to modify the structure of the AAPA to include the GOLD TFTs taught by Hatano. However, the essence of the present invention is to optimize the structure of TFTs that constitutes each circuit in response to the respective specifications of the pixel portion and the driver portion, by providing the LDD region so as to be overlapped, partially overlapped, or non-overlapped with the gate electrode. In n-channel TFTs of the driver portion, a first TFT has the LDD region that is overlapped with the gate electrode, a second TFT has the LDD region that is partially overlapped with the gate electrode, and/or a third TFT has the LDD region that is not overlapped with the gate electrode. Also, in a p-channel TFT (a fifth TFT) of the driver portion, the LDD region is not provided. Furthermore in the n-channel TFT (a fourth TFT) of the pixel portion, the LDD region is formed so as not to be overlapped with a gate electrode. In response to this rejection, the Applicants have amended the independent claims to expressly state the conductivity of each TFT.

Applicants appreciate that there are two types of semiconductor conductivity known as p-type and n-type that constitutes the driver circuitry. However, neither the AAPA nor Hatano suggest or teach arranging the above-mentioned LDD regions in response to the respective specifications of the conductivity (n-type/p-type) and the circuits (pixel/driver) in order to

prevent fluctuation of properties due to the kink effect or the hot electron effect, to reduce the off current value, and/or to make the switching operation reliable. (Please see the specification, Page 24, line 21, through page 35, line 14). Even if motivation were found to combine these prior art references, the Applicants respectfully submit that the structure of the present invention could not be anticipated.

For the reasons stated above, the Examiner has failed to set forth a *prima facie* case of obviousness; therefore, the Applicants respectfully request that the Examiner withdraw the § 103 rejections.

***Claims 2-8, 10-17, 19-26, 28-35, and 37-44 are Patentable Over the AAPA, Hitano and Either Mimura, Mikoshiba, Fukunaga, or Stewart***

Claims 2, 10-11, 19-20, 28-29, and 37-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Hatano as applied to claims 1, 9, 18, 27, and 36 above, and further in view of Mimura et al., U.S. Patent No. 6,127,210 (Mimura). Claims 3-4, 12-13, 21-22, 30-31, and 39-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Hatano as applied to claims 1, 9, 18, 27, and 36 above, and further in view of Mikoshiba, U.S. Patent No. 5,499,123 (Mikoshiba). Claims 5-7, 14-16, 23-25, 32-34 and 41-43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Hatano taken with Mikoshiba, as applied to claims 3, 12, 21, 30 and 39 above, and further in view of Fukunaga et al., U.S. Patent No. 5,706,064 (Fukunaga). Claims 81-85 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the AAPA in view of Hatano as applied to claim 1, 9, 18, 27 and 36 above, and further in view of Stewart, U.S. Patent No. 5,302,966 (Stewart).

Please incorporate the arguments above with respect to the deficiencies in the AAPA and Hitano. Mimura, Mikoshiba, Fukunaga, and/or Stewart do not correct the deficiencies in the AAPA and Hitano.

For the reasons stated above, the Examiner has failed to set forth a *prima facie* case of obviousness; therefore, the Applicants respectfully request that the Examiner withdraw the § 103 rejections.

***Conclusion***

Having responded to all rejections set forth in the outstanding non-final Office Action, it is submitted that the claims are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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Attachments: Marked-Up Version Of The Specification and Amended Claims

**MARKED-UP VERSION OF THE AMENDMENTS TO THE SPECIFICATION**

At Page 40, paragraph 3 to Page 41, replace with the following:

--Fig. 14C shows an example of the structure of a sampling circuit TFT. The n-channel TFT of this circuit is a single gate, and second impurity regions that become LDD regions [and overlap the gate electrode] are formed on both the source side and the drain side. The length of the LDD regions 205 and 206 which do not overlap the gate electrode may be formed in the range of 0.5 to 3.0 $\mu$m, and both are preferably made of equal length. The objective of lowering the off current value, and the objective of preventing degradation of the TFT due to the hot carrier effect, can both be achieved at the same time by these LDD regions.

Fig. 14D is a structure suitable to a driver circuit operated at a high speed by a driver voltage of approximately 1.5 to 5 V. Third impurity regions that overlap the gate electrode are not formed [in] at the side of a drain region 208 of the n-channel TFT, and this becomes a structure that prevents reduction of the operational frequency due to a parasitic capacity.--

**MARKED-UP VERSION**
**OF THE AMENDED CLAIMS**

1. (Amended) A semiconductor device comprising a driver circuit and a pixel section [comprising thin film transistors] over a substrate, wherein:

a) said driver circuit includes:

a first thin film transistor comprising:

a channel forming region and a third impurity region having [a conductivity type] n-type conductivity, formed on the inside of a gate electrode; and

a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region [having inverse conductivity type to said conductivity type]; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode.

2. (Amended) A semiconductor device according to claim 1, wherein:

an impurity element having [said conductivity type] the n-type conductivity is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

9. (Amended) A semiconductor device comprising a driver circuit and a pixel section [comprising thin film transistors] over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having [a conductivity type] n-type conductivity, formed on the inside of a gate electrode; and

a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode;

a second thin film transistor comprising:

a channel forming region and a third impurity region having [said conductivity type] the n-type conductivity, formed on the inside of a gate electrode; and

a second impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region [having an inverse conductivity type to said conductivity type]; and

b) said pixel section comprises:

a fourth thin film transistor having:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region [having said conductivity type], formed on the outside of the gate electrode.

10. (Amended) A semiconductor device according to claim 2, wherein:

an impurity element having [said conductivity type] the n-type conductivity is included in the third impurity region and in the fourth impurity region; and

a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

11. (Amended) A semiconductor device according to claim 9, wherein:

an impurity element having [said conductivity type] the n-type conductivity is included in the second impurity region and in the third impurity region; and

a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.

18. (Amended) A semiconductor device comprising a driver circuit and a pixel section [comprising thin film transistors] over a substrate, wherein:

a) said driver circuit comprises:

[a first thin film transistor comprising:]

[a channel forming region and a third impurity region having a conductivity type, formed on the inside of a gate electrode; and]

[a first impurity region having said conductivity type which forms a source region or a drain region, formed on the outside of the gate electrode;]

a third thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a second impurity region having [said conductivity type] n-type conductivity, and a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region, and a fifth impurity region having p-type conductivity which forms a source region or a drain region [having an inverse conductivity type to said conductivity type]; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region [having said conductivity type], formed on the outside of the gate electrode.

19. (Amended) A semiconductor device according to claim 18, wherein:

[an impurity element having said conductivity type is included in the third impurity region and in the fourth impurity region; and]

[a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.]

a length of said second impurity region is 0.5 to 3.0 μm.

20. (Amended) A semiconductor device according to claim 18, wherein:

[an impurity element having said conductivity type is included in the second impurity region and in the third impurity region; and]

[a concentration of the impurity element included in said second impurity region is the same as a concentration of the impurity element included in said third impurity region.]

said third and fifth thin film transistor constitute a sampling circuit.

27. (Amended) A semiconductor device comprising a driver circuit and a pixel section [comprising thin film transistors] over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having [a conductivity type] n-type conductivity, formed on the inside of a gate electrode; and

a first impurity region having [said conductivity type] the n-type conductivity which forms a source region or a drain region, formed on the outside of the gate electrode;

wherein said first thin film transistor constitutes a shift register circuit, and

a second thin film transistor comprising:

a channel forming region and the third impurity region having [said conductivity type] the n-type conductivity, formed on the inside of a gate electrode; and

a second impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region [having said conductivity type], formed on the outside of the gate electrode;

wherein said second thin film transistor constitutes a sampling circuit, and

[a third thin film transistor comprising:]

[a channel forming region formed on the inside of a gate electrode; and]

[a second impurity region having said conductivity type, and a first impurity region which forms a source region or a drain region having said conductivity type, formed on the outside of the gate electrode; and]

[a fifth thin film transistor comprising:]

[a channel forming region, and a fifth impurity region which forms a source region or a drain region having an inverse conductivity type to said conductivity type; and]

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region formed on the inside of a gate electrode; and

a fourth impurity region having [said conductivity type] the n-type conductivity, and a first impurity region having the n-type conductivity which forms a source region or a drain region [having said conductivity type], formed on the outside of the gate electrode.

36. (Amended) A semiconductor device having a panel comprising a pixel section and a driver circuit formed over a substrate, wherein:

a) said pixel section comprises a thin film transistor comprising:

a semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said semiconductor layer and a gate electrode over said gate insulating film;

a channel forming region formed in said semiconductor layer;

a source region and a drain region formed in said semiconductor layer; and

a lightly doped drain (LDD) region, formed in said semiconductor layer [to exclude the region underneath said gate electrode] so as not to be overlapped with said gate electrode, and

b) said driver circuit comprises:

a first thin film transistor comprising:

a first semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said first semiconductor layer and a first gate electrode over said gate insulating film;

a first channel forming region formed in said semiconductor layer;

a first source region and a first drain region formed in said first semiconductor layer; and

a first lightly doped drain (LDD) region, formed in said first semiconductor layer [provided in a portion underneath] so as to be overlapped with said first gate electrode, and

a second thin film transistor comprising:

a second semiconductor layer formed over an insulating surface of said substrate;

a gate insulating film on said second semiconductor layer and a second gate electrode over said gate insulating film;

a second channel forming region formed in said second semiconductor layer;

a second source region and a second drain region formed in said second semiconductor layer; and

a second lightly doped drain (LDD) region, formed in said second semiconductor layer [to exclude the region underneath with said second gate electrode: and] so as to be partially overlapped with said second gate electrode.

[a third thin film transistor comprising:]

[a third semiconductor layer formed over an insulating surface of said substrate;]

[a gate insulating film on said third semiconductor layer and a third gate electrode over said gate insulating film;]

[a third channel forming region formed in said third semiconductor layer;]

[a third source region and a third drain region formed in said third semiconductor layer;]

[a third lightly doped drain (LDD) region formed in said third semiconductor layer provided in a portion underneath said third gate electrode, and]

[a fourth lightly doped drain (LDD) region, formed in said third semiconductor layer to exclude the region underneath said third gate electrode.]